Precision second-order sigma-delta modulator for energy metering applications IRL5103FI

General Description

A precision, second-order, Σ-Δ modulator for energy metering applications that monitor shunt voltages and require galvanic isolation.

The fully integrated power isolation allows operation from a single 3.3 V power supply which makes the device best suited for use in confined spaces.

The on-chip digital isolation allows the both sides of the system to operate at different common-mode voltages and protect the low-voltage part from hazardous damage.

The device accepts both differential and single-ended input signal of ±50 mV and then converts it in a single-bit, high speed output stream with the data rate of 1 MHz. The original information can be reconstructed by using a digital filter like $sinc^3$ to achieve 80 dB signal-to-noise ratio (SNR) at 3.91 kSPS with a 256 decimation factor.

Applications

- Shunt-based electricity meters
- Isolated sensor interfaces
- Electrical motor drives
- Solar and wind power inverters
- Power monitoring applications
- Optocoupler replacement

Features

- 1 MHz master clock input frequency
- SNR 80 dB typical
- 16 bits, no missing codes
- ±50 mV peak input range
- 14 mA current consumption
- Single 3.3 V supply
- On board power and digital isolators
- 5000 VRMS isolation per 1 minute
- Capacitive isolation barrier with a working voltage of up to 690 V_{RMS}
- Temperature range of -40°C to +85°C
- 16-Lead SOIC Package or (optionally) DFN-16 Package

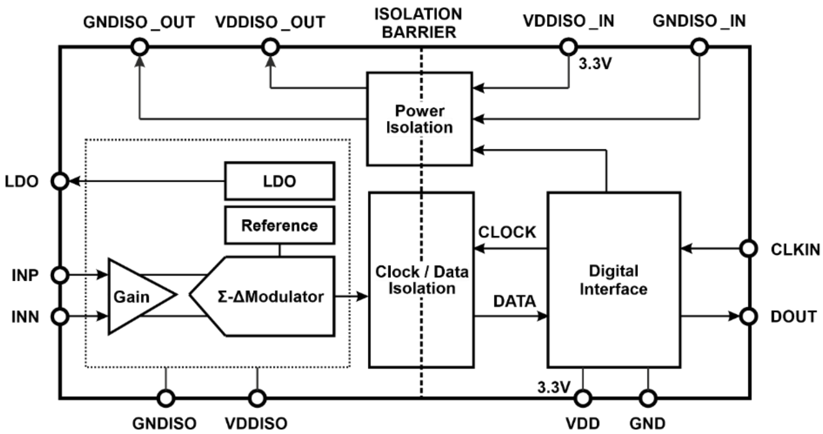

Figure 1 – Functional Block Diagram

Specifications

VDD = VDDISO_IN = 3.3 V ± 10%, GND = 0 V, on-chip reference, VINP = -50 mV to +50 mV, VINN = 0, CLKIN frequency = 1 MHz, tested with an external sinc3 filter, and a 256 decimation rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Temp	Unit
POWER SUPPLY					
VDDISO_IN/VDD to GNDISO_IN Pin	3.0	3.3	3.6	Full	V
Low-Voltage Side Supply Current		14	18	Full	mA
Output Voltage at VREF Pin	1.2		1.25	Full	V
Withstand Isolation Voltage (V_{ISO})		5000		25°C	V_{RMS}
ANALOG INPUTS					
Differential Input Voltage Range Between INP and INN Pins	-50		50	Full	mV
Single-Ended Input Voltage at INP or INN Pins	-50		50	Full	mV
Input Differential Impedance Between INP and INN Pins (DC)	1.6		2.8	Full	kOhm
ACCURACY					
Gain Error	-1		1	25°C	%
Offset Error	-0.15		0.15	25°C	mV
Input Referred Noise		1	5	Full	µV
Total Harmonic Distortion (THD)		-85		25°C	dBc
Signal-to-Noise Ratio (SNR)		80		25°C	dBc
INPUT CLOCK (CLKIN)					
Input Clock Frequency	0.9	1.0	1.1	Full	MHz
Input Clock Duty Cycle	45	50	55	Full	%
High Level Output Voltage	0.8·VDD			Full	V
Low Level Output Voltage			0.2·VDD	Full	V
High Level Input Current	-2		2	Full	mA
Low Level Input Current	-2		2	Full	mA
LOGIC PIN (DOUT)					
High Level Output Voltage	0.8·VDD			Full	V
Low Level Output Voltage			0.2·VDD	Full	V
High Level Input Current	-2			Full	mA
Low Level Input Current			2	Full	mA
Common-Mode Transient Immunity (CMTI)		20		25°C	kV/µs
Load Capacitance			30	Full	pF

Absolute Maximum Ratings

Table 2 – Absolute Maximum Ratings

Parameter	Rating
Electrical	
VDD, VDDISO_IN to GNDISO_IN	-0.3V to +4.0V
CLKIN to GNDISO_IN	-0.3V to +4.0V
INP, INN to GNDISO_IN	-0.3V to VDD+0.3V
Environmental	
Operating Temperature Range (Ambient)	-40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range	-65°C to +150°C
Electrostatic Discharge	
Human-body model (HBM)	±2000V

Typical Performance Characteristics

VDD = VDDISO_IN = 3.3 V ± 10%, GND = 0 V, on-chip reference, VINP = -50 mV to +50 mV, VINN = 0, CLKIN frequency = 1 MHz, tested with sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

Pin Configuration and Function Description

Functional Description

IC Architecture

The device is a fully differential, isolated Σ-Δ modulator which converts an analog input signal to a 1-MHz rate, single-bit data stream. The time average single-bit data from the modulator is directly proportional to the input signal.

The stream of digital ones and zeros at the modulator's output is transferred across a double capacitive silicon dioxide isolation barrier. Being separated from the secondary, high voltage side, the output data can be captured by a low-voltage microcontroller unit (MCU) for subsequent digital filtering and decimation.

The regulated power required for the modulator is provided by a fully integrated isolated dc-to-dc converter that eliminates the need for any external power isolation block. This power isolation uses an on-chip transformer separated with a thin-film polymer as an insulating material.

The both signal path and power separation result in a small form factor, total isolation solution.

Figure 2 shows a typical application circuit where a ±50 mV voltage at a current sensing resistor or a shunt, processed by the IR5103FI.

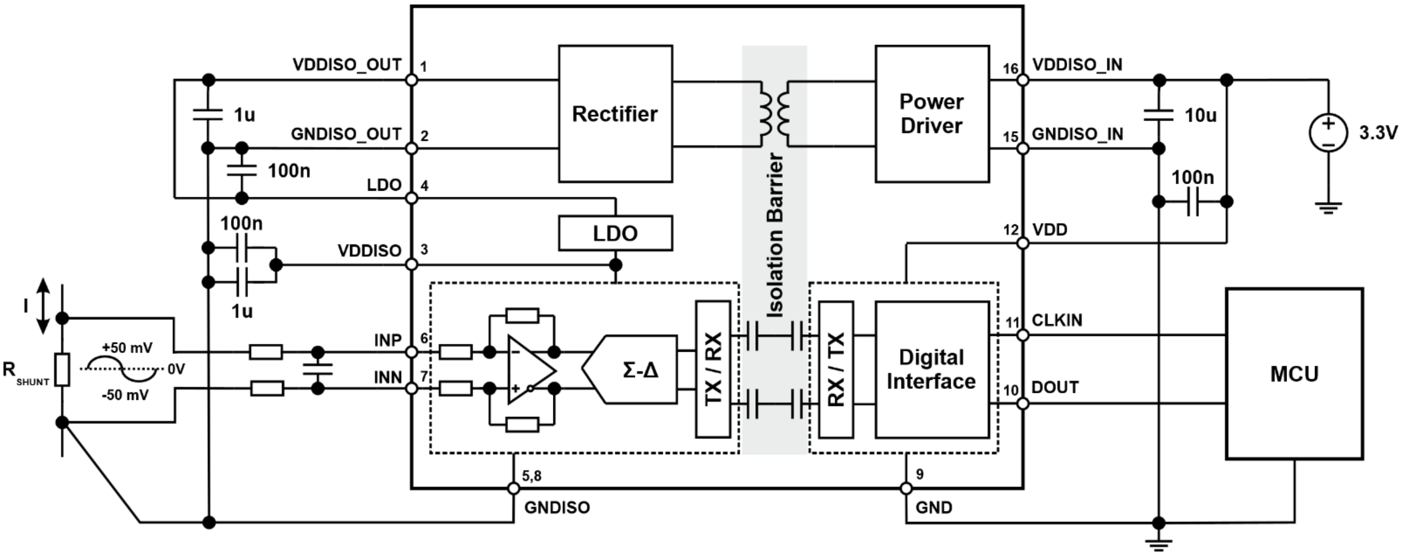

Figure 2 – Typical Connection Diagram

Analog Input Considerations

The fully differential operational amplifier buffers the analog inputs INP, INN from the switched-capacitor input stage of the Σ-Δ modulator. The gain needed for the overall signal path is set in the differential amplifier by internal precision resistors.

To reduce the offset and offset drift the differential amplifier is chopper-stabilized with the switching frequency set at one-sixteenth of the sampling frequency. The output spectrum of the modulator may contain spurs at this switching frequency and at its odd multiples.

The input voltages and input currents at pins INP, INN cannot exceed the range specified in the Absolute Maximum Ratings. The parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range and within the common-mode input voltage range.

In a typical case for directly measuring the voltage across a shunt resistor, the IR5103FI can be connected across the shunt resistor with a simple RC-low pass filter on each input.

Modulator

This circuit implements a second-order modulator stage that digitizes the input signal to a single-bit output stream. The externally supplied input clock (CLKIN) provides the clock signal for the sampling and conversion process as well as the output data interface.

The analog input signal is continuously sampled by the modulator and compared with an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter.

The modulator shifts the quantization noise to high frequencies. Therefore, a low-pass digital filter at the output of the device must be used to increase the overall performance. This filter also has to convert the single-bit data stream at a high data rate into a higher-bit data word at a lower rate (decimation).

The microcontrollers for electrical energy meters like MDR1206 have built-in hardware filters optimized for usage with the IR5103FI. Alternatively, a microcontroller from other vendors which offer a suitable programmable digital filter or a field-programmable gate array (FPGAs) can be used to implement the filter.

Voltage Reference

The device contains an internal voltage reference which is used for the modulator. The nominal reference voltage is 1.2 V. Its value drifts slightly with temperature as shown in Figure 3.

Because the on-chip dc-to-dc converter cannot supply external loads, this reference voltage cannot be overdriven by a standalone external voltage reference.

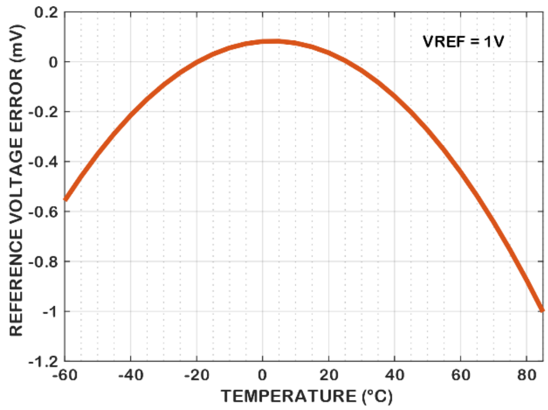

Figure 3 – Typical VREF Drift

Digital Output

A differential input signal of 0 V ideally results in a stream of alternating digital ones and zeros at the DOUT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 50 mV produces a stream of ones and zeros that are high 89% of the time. A differential input of -50 mV produces a stream of ones and zeros that are high 11% of the time.

These input voltages are within the specified linear range of the IR5103FI. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases.

The output of the modulator clips with a constant stream of all ones with an input greater than or equal to 56 mV. The output of the modulator clips with a constant stream of all zeros with an input less than -56 mV.

The timing diagram of the device operation is presented in Figure 4. Data outputs are available at the DOUT pin one propagation delay t_{PD} after the rising edge of the clock signal CLKIN.

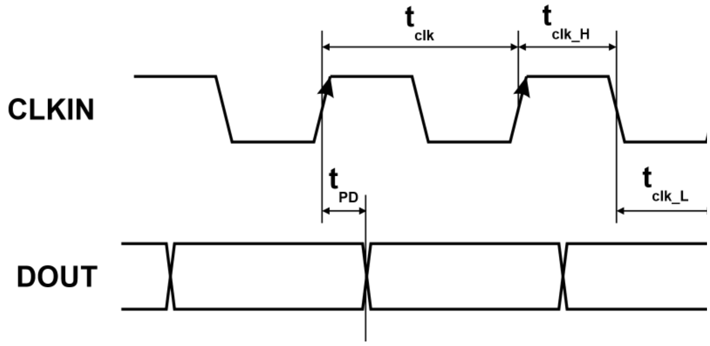

Figure 4 – Data Timing Diagram

Power management

The IR5103FI requires a single 3.3 V supply on its low-voltage side. This primary side is supplied directly through the VDD pin.

The secondary, high-side supply is internally generated by an integrated dc-to-dc converter. VDDISO_IN power is supplied to an oscillating circuit that drives the primary side of an air-cored, chip-scaled transformer. Power is then transferred to the secondary side, where it is rectified to a dc voltage of 4 – 6 V, which is output to the VDDISO_OUT pin. This voltage must be capacitively filtered externally and supplied back to the LDO pin of the chip. Here this rectified voltage is completely stabilized by an internal LDO, which produces the isolated power supply VDDISO. This supply voltage is intended to provide high analog performance of the signal path, so it cannot be used to power external circuitry.